TAIWAN SEMICONDUCTOR

AN-1010

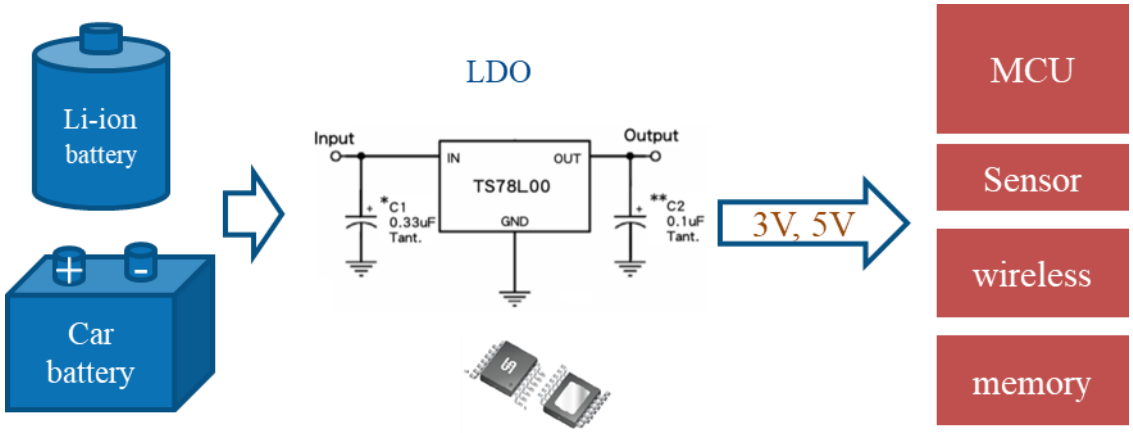
Low Dropout (LDO) regulator index and feature - application note

Content

1. Low Dropout (LDO) regulator introduction

1.1 Why needing Low Dropout (LDO) regulator

Low Dropout (LDO) regulator is suitable for low voltage difference provide close voltage regulation like 5V to 3V, the output voltage remains stable in spite of input voltage variation. Low Dropout (LDO) regulator is easy to use with less external components. LDO operate no noise to offer good voltage ripple suppression, it could provide automotive clean and reliable power (Figure 1).



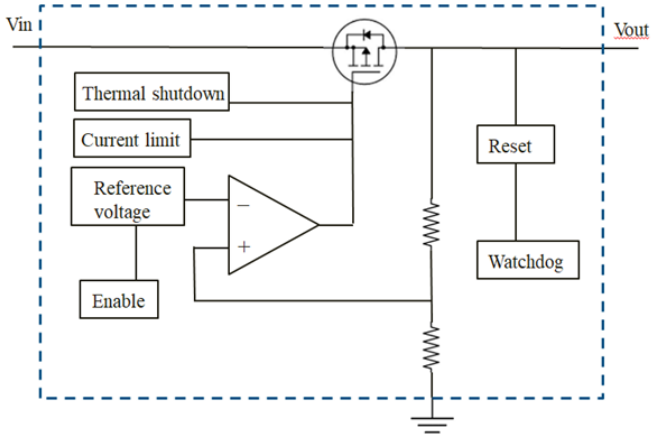
(Figure 1 – LDO application diagram)

1.2 Low Dropout (LDO) regulator concept

Low Dropout (LDO) regulator can regulate voltage if Vin close to Vout as formula:

$$V_{OUT} = V_{in} - V_{drop}$$

Low Dropout (LDO) regulator utilized switch element (Mosfet) working in liner region to regulate voltage, as a variable resistance (Figure 2).

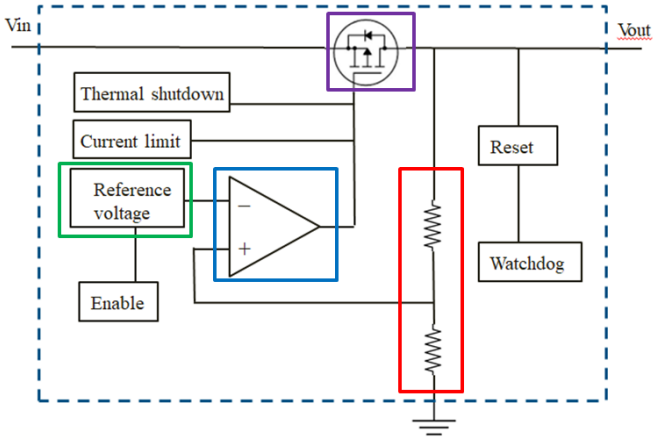


(Figure 2 – LDO block diagram)

1.3 LDO architecture

Low Dropout (LDO) regulator main circuit composition includes four portions (Figure 3):

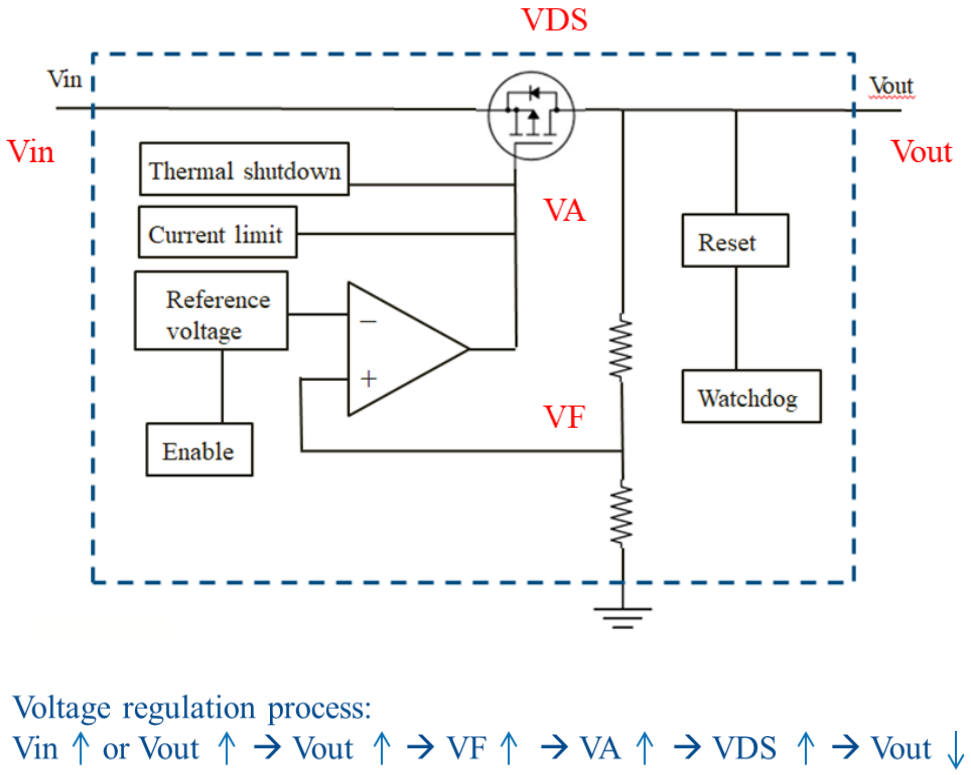
1. Feedback resistors: Two resistors composed, it is responsible for sampling Vout variation
2. Reference voltage: it provides accurate voltage for operation amplifier comparison reference
3. Operation amplifier: It compares feedback voltage with reference voltage to control switch device operation
4. Switch device: operate in linear region as a variable resistors to maintain Vout



(Figure 3 – LDO main composition)

1.4 LDO voltage stabilize concept

Low Dropout (LDO) regulator process voltage program: Once Vin increase or Vout increase, the feedback resistance will sense Vout and make VF increase. Operation amplifier compares VF with reference voltage and provide signal and make VA increase. The switch device belongs P-MOSFET, the V_{DS} will increase when V_{GS} increase. So Vout will decrease to compensate the beginning Vout raising (Figure 4).



(Figure 4 – LDO voltage stabilize process procedure)

2. Low Dropout (LDO) regulator key index

2.1 Dropout voltage

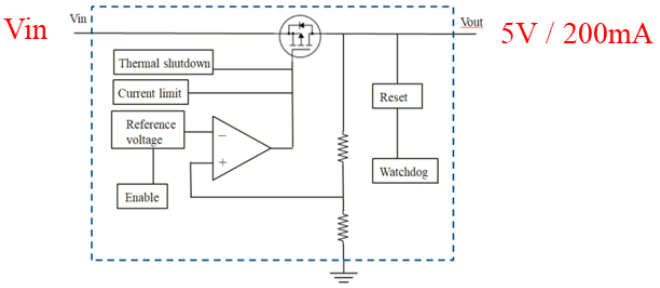
Dropout voltage Vdr is the minimum voltage difference of Vin and Vout, the demand voltage when Vin regulate to Vout as following formula:

$$V_{out} = V_{in} - V_{dr}$$

$$V_{in} \geq V_{out} + V_{dr}$$

Take TQL820CA14V50 datasheet as example (Figure 5). What is the Vin minimum needs to apply if we need to regulate to Vout=5V, Iout=200mA, the calculation is as below:

$$V_{in} \geq V_{out} + V_{dr} = 5V + 0.34V = 5.34V$$



TQL820CA14V50 datasheet:

ELECTRICAL SPECIFICATIONS (V_{IN} = 13.5V, T_J = -40 to 150°C unless otherwise noted)						
PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage						
Output Voltage	0.05mA < I_{OUT} < 200mA 5.44V < V_{IN} < 28V	V_{OUT}	4.9	5	5.1	V
Output Voltage	0.05mA < I_{OUT} < 100mA 5.27V < V_{IN} < 40V	V_{OUT}	4.9	5	5.1	V
Start-up Slew-rate	V_{IN} > 18V/ms, C_{OUT}=1µF 0.5V < V_{OUT} < 4.5V	dV_{OUT}/dt	--	35	--	V/ms
Current Limit	0V < V_{OUT} < 4.8V	I_{lim}	--	320	--	mA
Load Regulation	I_{OUT} = 0.05 to 200mA V_{IN} = 6V	$\Delta V_{OUT,lo}$	-15	-1.5	5	mV
Line Regulation	V_{IN} = 8 to 32V I_{OUT} = 1mA	$\Delta V_{OUT,li}$	-20	0	20	mV
Dropout Voltage (V_{dr}=V_{IN}-V_{OUT})	I_{OUT} = 200mA	V_{dr}	--	110	340	mV
Dropout Voltage (V_{dr}=V_{IN}-V_{OUT})	I_{OUT} = 100mA	V_{dr}	--	70	170	mV

(Figure 5 – Vdr datasheet description of TQL820CA14V50)

2.2 Thermal dissipation

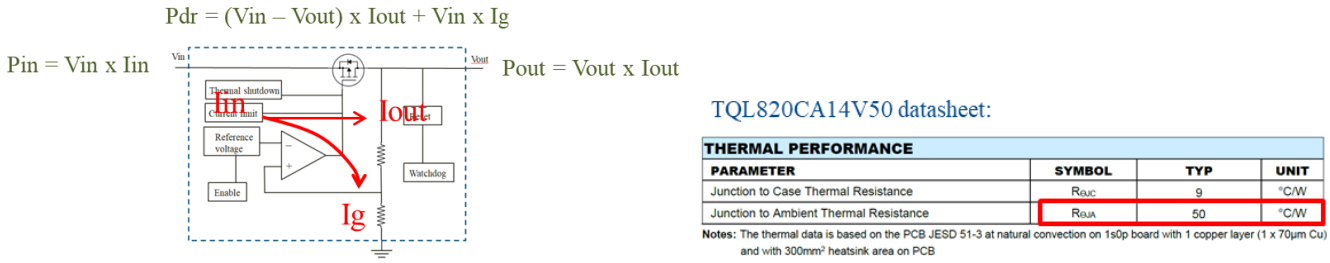
LDO regulate voltage by changing resistance of the switch element, there will be power dissipation in LDO and the power will turn to heat. We need to make sure the heat have to be less than LDO junction temperature.

Take TQL820CA14V50 datasheet as example (Figure 6). Determine temperature affect LDO calculation:

1. Iin = Iout + Ig (ground current)

2. LDO power dissipation: Pdr = (Vin – Vout) x Iout + Vin x Ig

3. Judge TA + (RthjA x Pdr) < Tj (LDO junction temperature)



THERMAL PERFORMANCE			
PARAMETER	SYMBOL	TYP	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	9	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	50	°C/W

Notes: The thermal data is based on the PCB JESD 51-3 at natural convection on 1s0p board with 1 copper layer (1 x 70μm Cu) and with 300mm² heatsink area on PCB

(Figure 6 – RthjA datasheet description of TQL820CA14V50)

2.3 Quiescent current

Iq (quiescent current): When external current is zero, LDO consume current for internal circuits – bandgap reference voltage, operation amplifier, output diver, current limit, thermal shutdown, watchdog... Low Iq contribute low standby power dissipation, it is important for long standby mode application in battery– smartwatch, cellphone, health tracker...

2.4 PSRR

Power supply ripple rejection (PSRR) represents noise ratio of input noise couples into output noise. LDO can clean some input noise, then output minimal ripple with below decibel formula:

$$\mathrm{PSRR(dB)} = 20\log(\frac{Vin(ripple)}{Vout(ripple)})$$

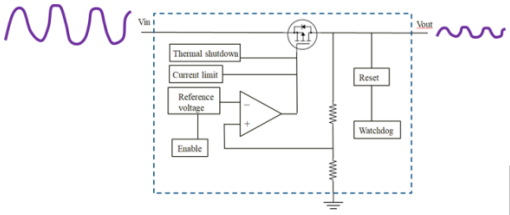
Take TQL820CA14V50 datasheet as example (Figure 7). If Vin with ripple voltage 50mV, what is the Vout ripple voltage LDO can suppress:

Ex: If vin (ripple) = 50mV

59dB =20 log(50mV/($Vout$ ($ripple$)))

891 = 50mV/($Vout$($ripple$))

Vou($ripple$ = 56.1uA



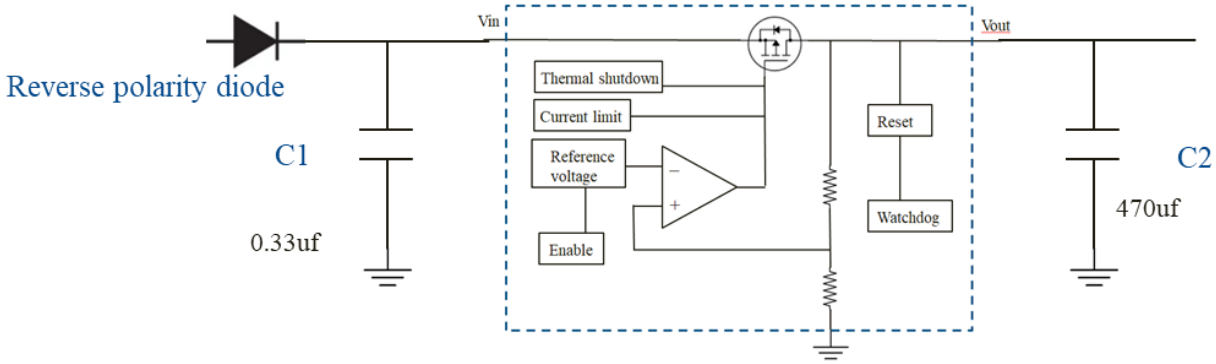
TQL820CA14V50 datasheet:

Power Supply Ripple Rejection	f = 100Hz V = 0.5Vpp	PSRR	--	59	--	dB

(Figure 7 – PSRR datasheet description of TQL820CA14V50)

3. Low Dropout (LDO) regulator application circuit

Vin connect capacitance C1 in series, it could prevent voltage self-exciting oscillation by harness wire inductance effect. Vout connect capacitance C2, it could prevent voltage ripple. In reverse polarity situation, surge current would flow through switch device. Connect reverse polarity diode in series to protect is mandatory (Figure 8).



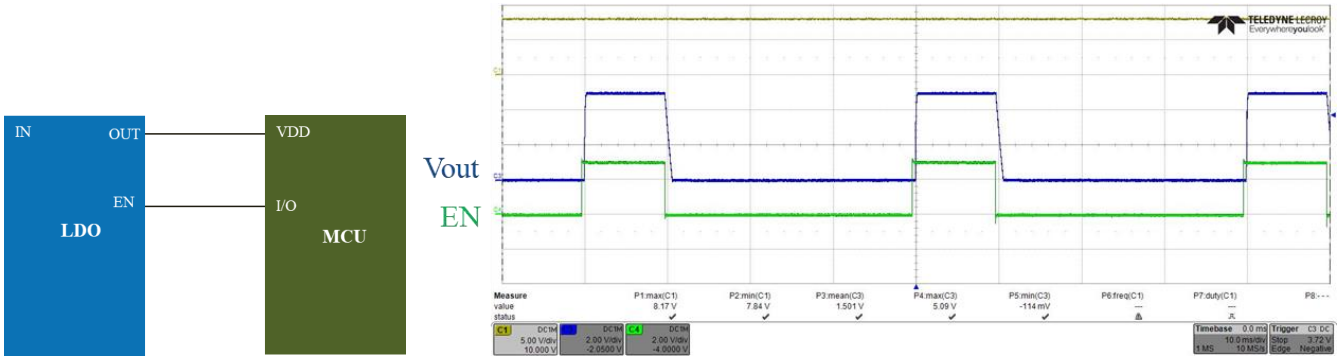
(Figure 8 – LDO circuit application diagram)

4. Low Dropout (LDO) regulator embedded function

LDO main function is voltage regulation. For integrated circuit concept, LDO also integrate additional functions for application demand.

4.1 Enable

Battery connected to LDO system still consume power in standby mode, MCU could control LDO operation via Enable function to gain the battery power efficiency. Take TQL820CA14V50 as example: EN pin receive low-logic signal from MCU to turn off LDO Vout; oppositely EN pin receive high-logic signal to turn on LDO Vout (Figure 9).



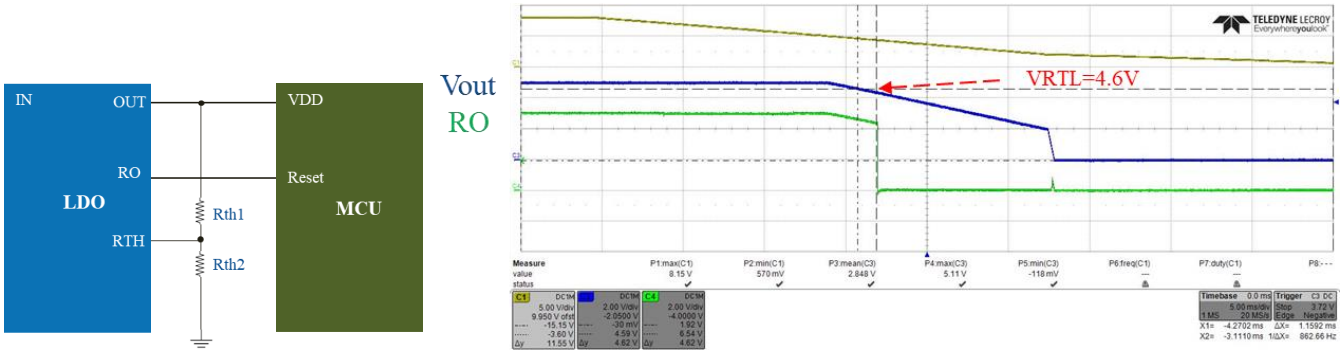
(Figure 9 – Enable function operation waveform)

4.2 Under voltage reset

Once MCU powered unstable low voltage, it might operate incorrect logic operation. Take TQL820CA14V50 as example: LDO could monitor its Vout if lower to reset lower threshold voltage VRTL (ex. TQL820CA14V50 typ. VRTL = 4.6V), LDO RO pin will provide low-logic signal to reset MCU (Figure 10). VRTL could be adjusted by connecting external resistor Rth1 and Rth2:

$$V_{RTL,new} = V_{RTTH} \times (R_{th1} + R_{th2})/R_{th2}$$

$$V_{RTTH}\ is\ adjustment\ threshold (\text{ex. TQL820CA14V50 typ.} V_{RTTH} = 1.2\text{V})$$

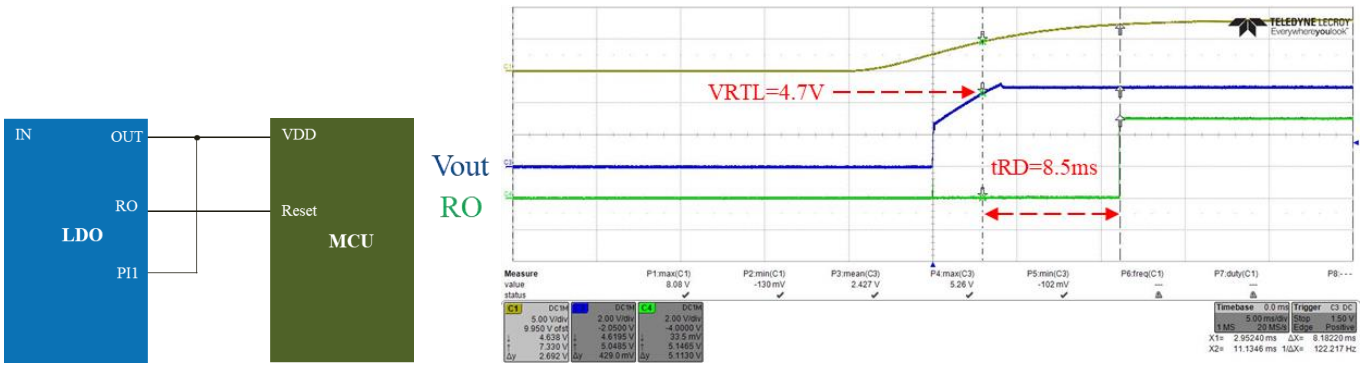


(Figure 10 – Under voltage reset operation waveform)

4.3 Power on delay reset

MCU oscillator needs 1 – 10ms to be stable while power on. If MCU start working before oscillator stale, MCU might initialize incorrectly. LDO power on reset delay time can prevent MCU initialize before oscillator is stable. Take TQL820CA14V50 as example: When Vout exceeding reset upper threshold voltage VRTH (ex. TQL820CA14V50 typ. VRTH = 4.7V), LDO RO pin will delay reset time (tRD = 8.5ms when PI1 connect Vout) to switch low-logic signal to high-logic signal (Figure 11). The timing tRD can be controlled by PI1 pin.

PI1 connected to	t_{RD}
GND	16.5ms
OUT	8.5ms

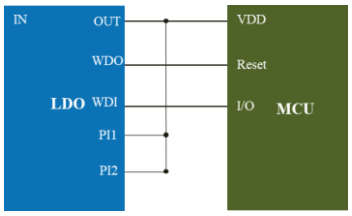


(Figure 11 – Power on delay reset operation wave form)

4.4 Watchdog

Watchdog timer is an important function to monitor MCU operation, watchdog monitor MCU signal timing periodically. Once MCU provide no expected signal timing, watchdog will reset MCU. Take TQL820CA14V50 as example: Watchdog timer WDO pin start by an high-logic signal time of tWDI,i (ignore time, ex. TQL820CA14V50 typ. tWDI,i = 16ms), then remain time of tWDI,tr (trigger time, ex. TQL820CA14V50 typ. tWDI,tr = 16ms when PI1, PI2 connect Vout) to monitor MCU signal exist in this period or not. If there is no MCU signal within tWDI.tr, WDO will provide low-logic signal to reset MCU among 8ms. The Watchdog Trigger Time is programmable with PI1 and PI2. The timing selection as follows:

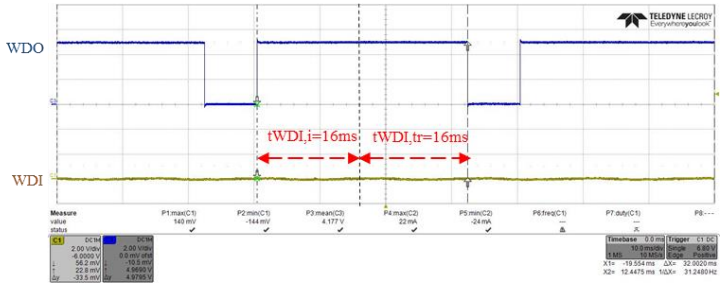
PI1 connected to	PI2 connected to	$t_{WDI,tr}$
GND	GND	96ms
OUT	GND	48ms
GND	OUT	32ms
OUT	OUT	16ms



Operation example 1:

Select Watchdog Trigger Time tWDI,tr = 16ms

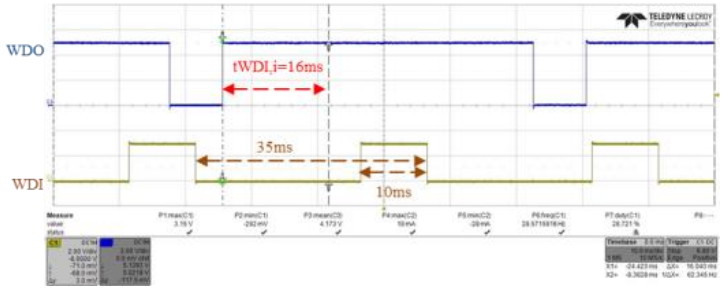
1. No signal apply to WDI
2. All pulse falling edge signal all within tWDI,tr
3. WDO no provide low-logic signal

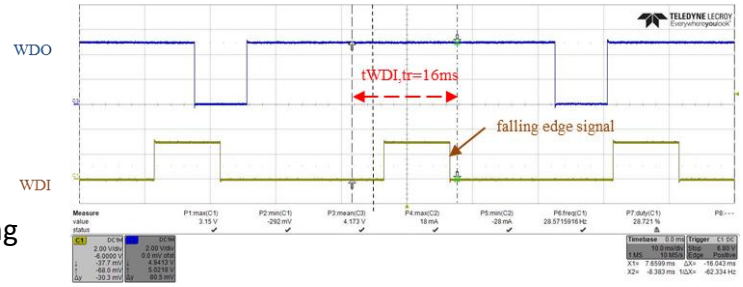


Operation example 2:

Select Watchdog Trigger Time tWDI,tr = 16ms

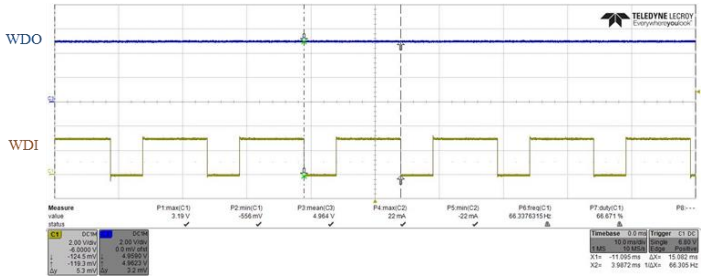
1. Apply to WDI (pulse 10ms/ width 35ms)
2. WDO start counting tWDI,i = 16ms
3. All WDI received falling edge signal within tWDI,i is ignored
4. After tWDI,i finished, start counting tWDI,tr=16ms
5. Find out WDI falling edge signal with tWDI,tr
6. Continue counting tWDI,tr
7. There is no WDI falling edge signal within tWDI,tr, WDO switch to low-logic signal among 8ms to reset MCU





Operation example 3:

Select Watchdog Trigger Time tWDI,tr = 16ms
1. Apply WDI (pulse 10ms/ width 15ms)
2. All pulse falling edge signal all within tWDI,tr
3. WDO no provide low-logic signal



4.5 Thermal shutdown

Thermal shutdown: Take TQL820CA14V50 as example will shut down once internal sense 160C; it automatically restart after internal temperature back to 130C.

4.6 Current limit

Current limit: To avoid of output short circuit to ground, Take TQL820CA14V50 as example limits output current from damage by excessive power dissipation.

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